

REMARKS

This is in response to the Office Action mailed June 27, 2002. Applicant acknowledges the allowance of claims 1 - 28, and the allowability of claim 30 if rewritten in independent form.

Claim 30 has been rewritten according to the Examiner's suggestion to place the case in condition for allowance. Claims 29 and 30 - 31 have been cancelled, without prejudice.

Claim 31 is being cancelled to expedite processing of the application, as it is not agreed that Williams, U.S. Patent No. 4,873,757 discloses, in combination with the structure recited in cancelled claim 29, "an electrically conductive trace contained between two of said layers of dielectric sheets, said electrically conductive trace communicating with said first set of electrically conductive windings." Williams does disclose any traces in addition to the windings themselves.

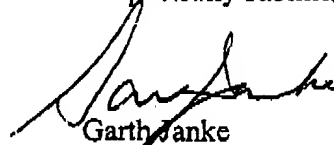
Claim 32 is also being cancelled to expedite processing of the application, as it is not agreed that Williams, U.S. Patent No. 4,873,757 discloses, in combination with the structure recited in cancelled claim 29, "at least one component secured to an exterior surface of said multilayer printed circuit board at a location over said electrically conductive trace." Williams does not disclose any component mounted to its PWB 12, and, moreover, does not disclose where such a component would be secured.

In the "examiner's statement of reasons for allowance," selected features of selected claims are explicitly noted. However, both 35 USC §§102 and 103 refer to "the invention," and the invention is defined by all of the words in the claim taken as a whole. It is assumed, therefore, that the reasons for allowance should be interpreted as though use of the term "*inter alia*" is shorthand

for referring to all of the remaining words in the claims. For example, the reason for allowance of claim 1 is assumed to be shorthand for the following (and likewise for each of the remaining claims):

Claim 1 is patentable because the prior art of record does not teach or suggest a power processing device comprising: (a) a multilayer printed circuit board having multiple layers of dielectric sheets; (b) a first transformer having, a first core extending through said layers of dielectric sheets, and, a first set of electrically conductive windings, at least one of said windings of said first set of electrically conductive windings contained between two adjoining layers of said dielectric sheets; (c) a second transformer having, a second core extending through said layers of dielectric sheets, and, a second set of electrically conductive windings, at least one of said windings of said second set of electrically conductive windings contained between two adjoining layers of said dielectric sheets, and, (d) at least one electrically conductive trace extending between said first set of electrically conductive windings and said second set of electrically conductive windings, said at least one electrically conductive trace contained between two adjoining layers of said dielectric sheets.

Respectfully submitted,



Garth Janke
Reg. No. 40,662
(503) 228-1841

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MARKED UP VERSION OF AMENDMENTS**In the Claims:**

Cancel, without prejudice, claims 29 and 31 - 32.

Claim 30 has been amended as follows:

--30. [The power processing device according to claim 29, further including] A power processing device comprising:

a) a multilayer printed circuit board having multiple layers of dielectric sheets; and

b) a transformer having

1) a core extending through said layers of dielectric sheets, and

2) a first set of electrically conductive windings, at least one of said windings of said first set of electrically conductive windings contained between two adjoining layers of said dielectric sheets, and at least one of said windings positioned on an external surface of said

multilayer printed circuit board; and

a first shielding layer disposed on an exterior surface of said
multilayer printed circuit board.--